WHAT IS CLAIMED IS:

1. A semiconductor memory device having a multiport memory, comprising:

a plurality of memory cells arranged in columns and rows;

a plurality of first word lines each arranged corresponding to each row, electrically connected to said memory cell, and selected in accordance with an address signal from a first port when accessed from said first port; and

a plurality of second word lines each arranged corresponding to each row, electrically connected to said memory cell, and selected in accordance with an address signal from a second port when accessed from said second port, wherein

each of said plurality of first word lines and each of said plurality of second word lines are arranged alternately in a planar layout.

2. The semiconductor memory device according to claim 1, wherein respective planar layouts of transistors in two said memory cells adjacent to each other in a row direction in a same column are line-symmetric to each other with respect to a boundary line between said two memory cells.

3. The semiconductor memory device according to claim 1 further comprising an insulating layer arranged between said first word line and said second word line, wherein

one of said first word line and said second word line is arranged below said insulating layer, and the other of said first word line and said second word line is arranged above said insulating layer.

4. A semiconductor memory device having a content addressable memory, comprising:

a plurality of content addressable memory cells arranged in columns and rows;

a plurality of word lines each arranged corresponding to each row

and electrically connected to said content addressable memory cell; and

a plurality of match lines each arranged corresponding to each row and electrically connected to said content addressable memory cell, wherein

in a first row and a second row adjacent to each other, said word line in said first row and said word line in said second row are adjacent to each other, and in said second row and a third row adjacent to each other, said match line in said second row and said match line in said third row are adjacent to each other.

5. The semiconductor memory device according to claim 4 further comprising an insulating layer arranged between said word line and said match line, wherein

one of said word line and said match line is arranged below said insulating layer, and the other of said word line and said match line is arranged above said insulating layer.